

FIG. 1

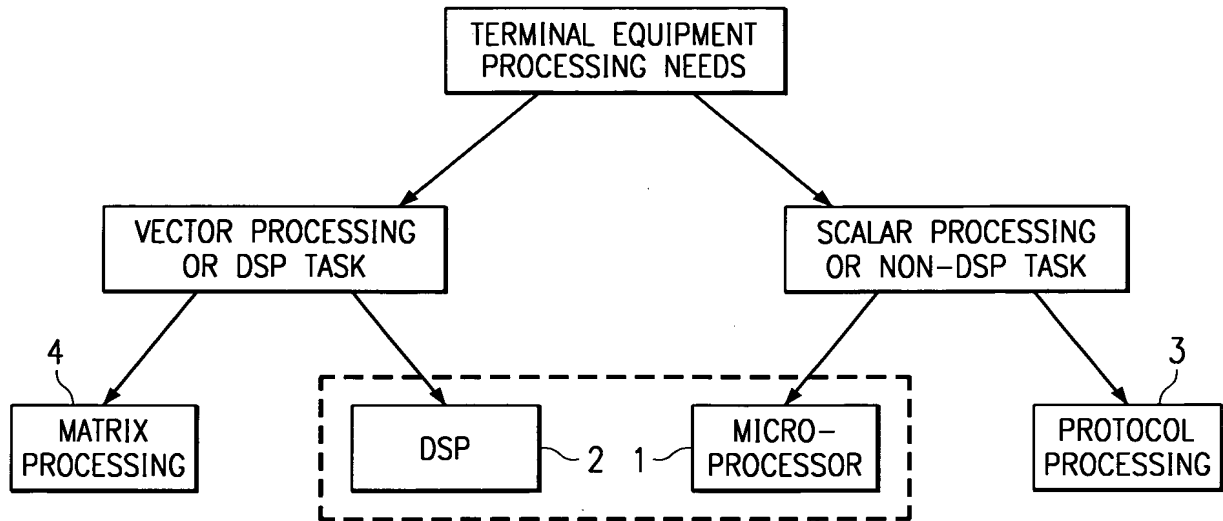
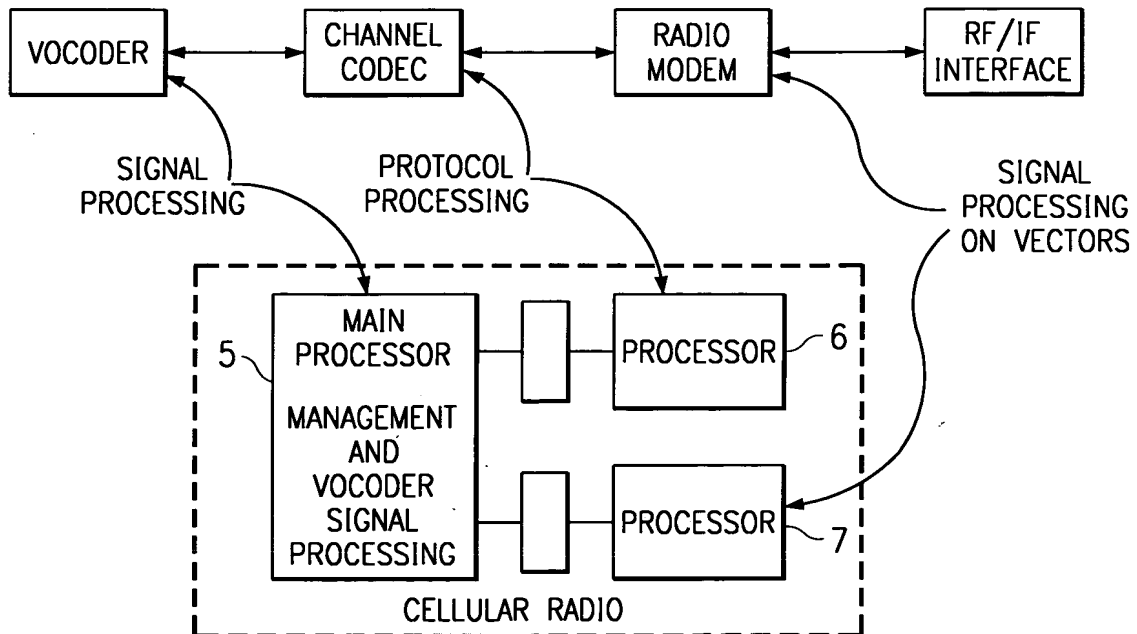


FIG. 2



*FIG. 3*

PERFORMANCE OF CHANNEL CODEC ROUTINES

ROUTINES	DSP UTILIZATION C5x	PROC PROTOCOL PP UTILIZATION
16 BIT CRC IDENTIFICATION	6 INSTR/BIT 5 INSTR/BIT	4 INSTR/BIT 1 INSTR/BIT
RATIO		
SEL/INSTR EFFICIENCY NO. OF TRANS MIPS	x1 58 KTx 28 MIPS	x2.2 6.5 KTx 28x2.2=62 MIPS DSP

*FIG. 4*

PERFORMANCE OF MODEM ROUTINES

ROUTINES	DSP UTILIZATION C5x	ARRAY PROC
METRIC COMPUTATION 57 SYMBOLS (4 SAMPLES)	43800 CYCLES	4400 CYCLES
RATIO		
INSTRUCTION SETTING EFFICIENCY MIPS	x1 28 MIPS	x10 28x10=280 MIPS DSP

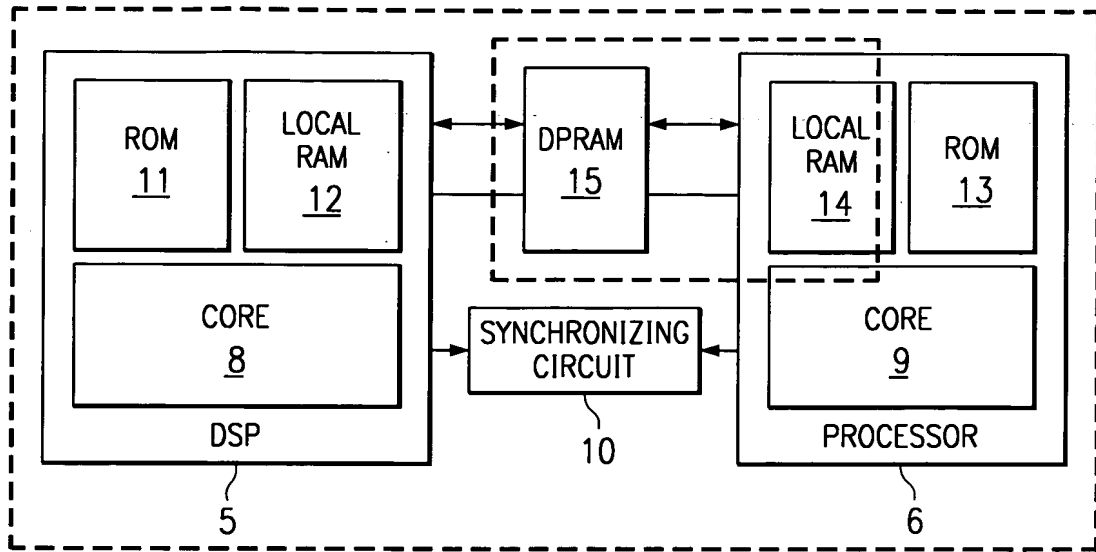


FIG. 5

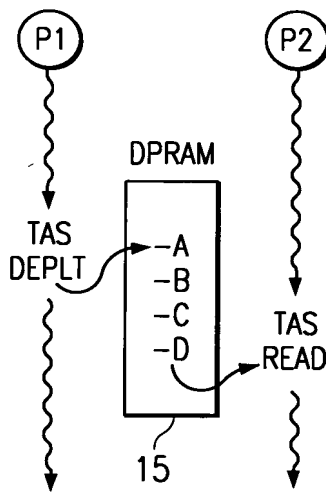


FIG. 6

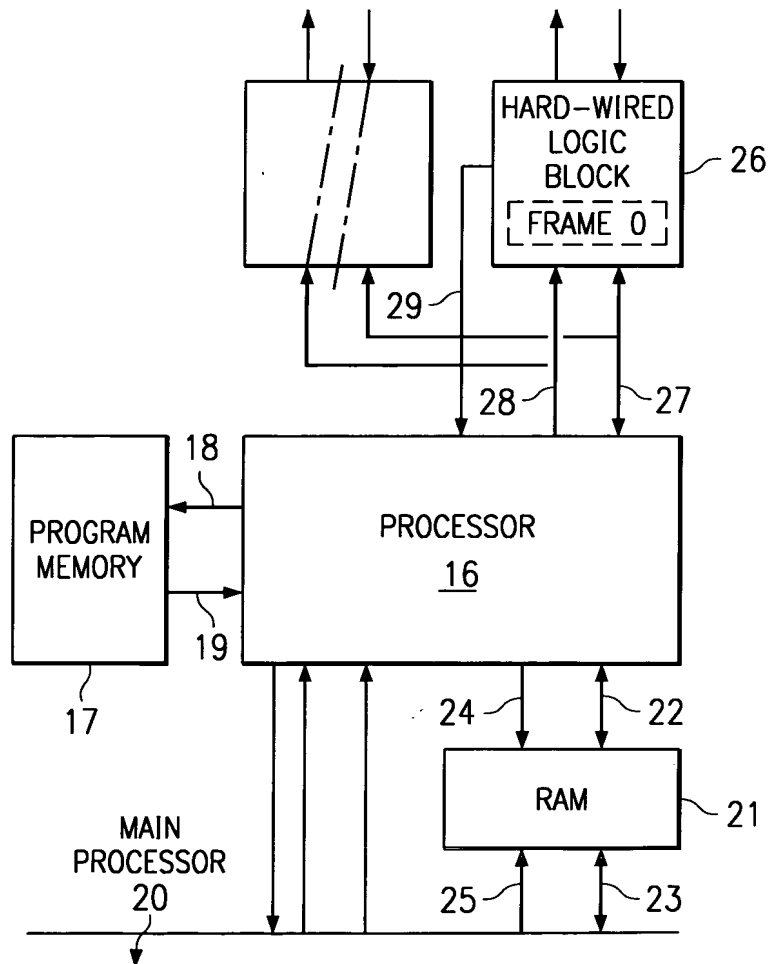


FIG. 7

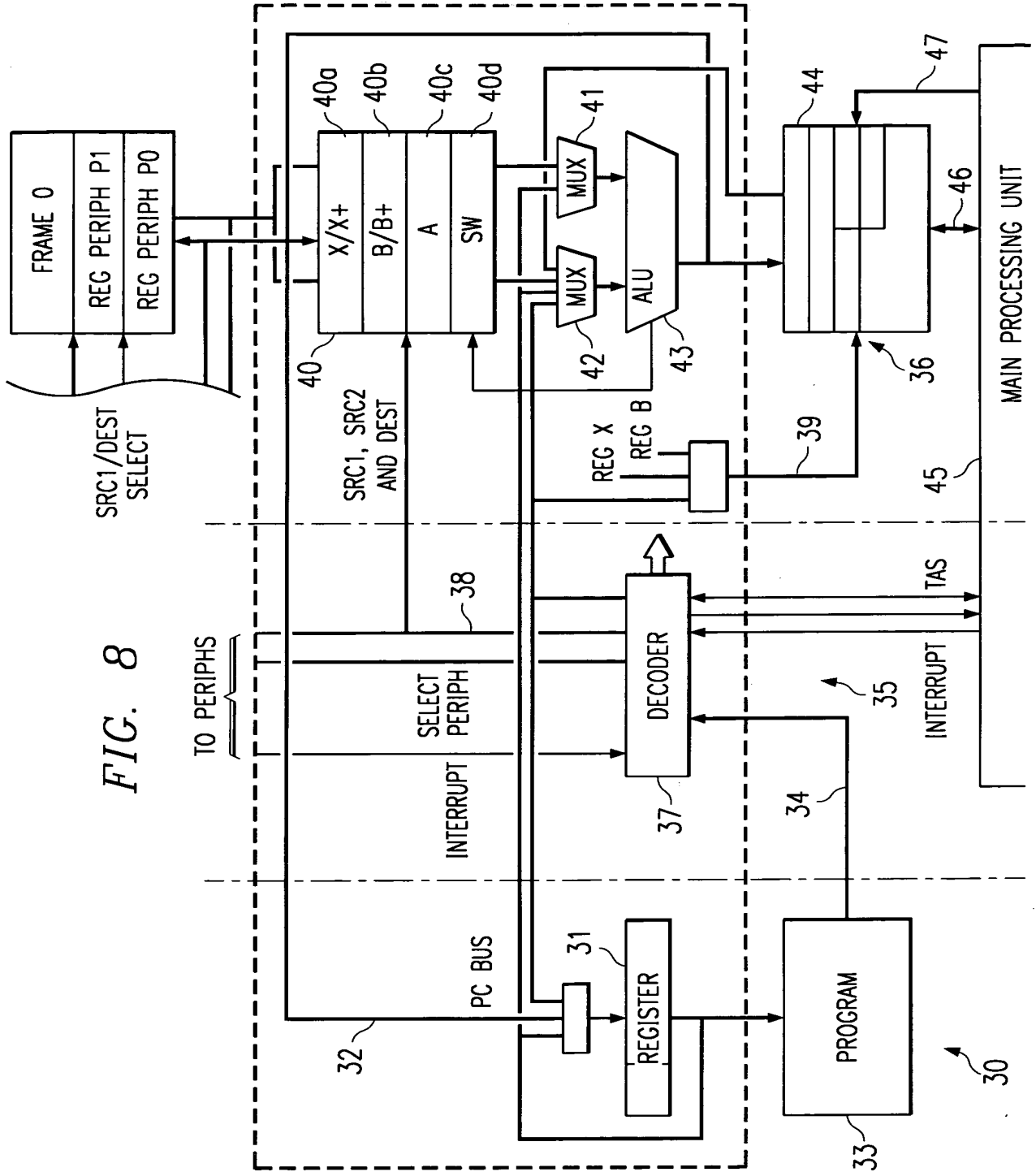


FIG. 9

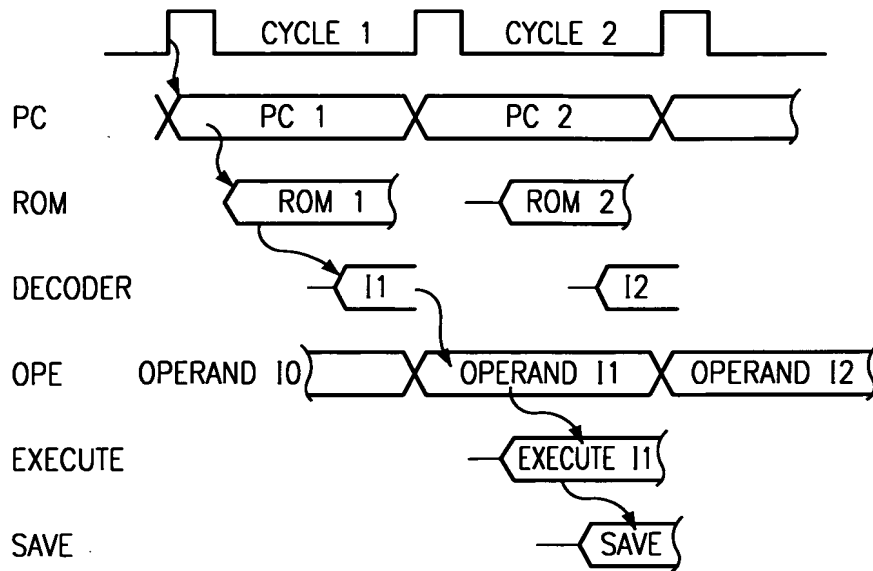


FIG. 11

OP CODE														
TYPE														
0	0 0	ALU	Cc	1	K	W	Rm	K						} INTEGER/ TRANSFER
1	0 1	ALU	Cc	1	DMA	W	Rm	DMA				L		
2	1 0	ALU	Cc	1	@	+	W	Rm	Rn	FP	S	L		
3	1 1	CODE	Cc		@	D	W	PMA						} MONITORING
4	1 1	CODE	Cc		@	+	W		Rn					

FIG. 10

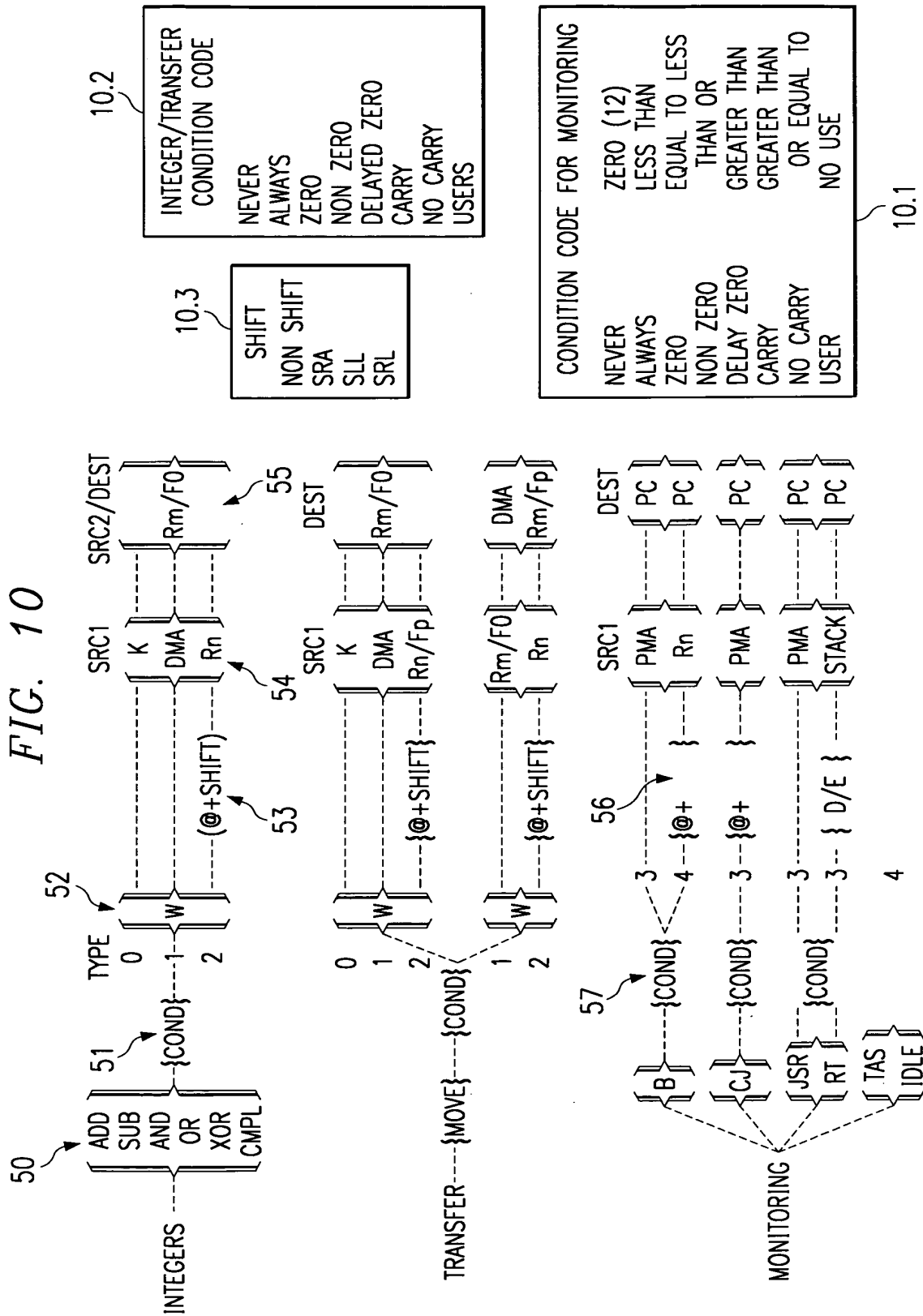


FIG. 12

ALU	CODE	Cc	
0 - SUB	0 - ST TYPE 1	0 - NEVER	8 - Z12
1 - CPL	1 - ST TYPE 2	1 - ALWAYS	9 - LO
2 - ADD	2 - B TYPE 3	2 - Z	10 - LE
3 - AND	3 - B TYPE 4	3 - NZ	11 - G
4 - OR	4 - CALL	4 - ZD	12 - GE
5 - XOR	5 - RTS	5 - C	13 - NU
6 - PASSA	6 - RTI	6 - NC	14 - (BL)
7 - SUBC	7 - STOP	7 - USER	15 -

Rm/Rn	W	L	S
0 - P0	0 - R/W BYTE	0 - Rm LOW	0 - PASS
1 - P1	1 - R/W WORD	1 - Rm HIGH	1 - SRA
2 - A			2 - SLL
3 - B			3 - SRL
4 - X			
5 - PC			
6 - SW			
7 - SP			

L
0 - DMA/Rn LOW
1 - DMA/Rn HIGH

FIG. 14

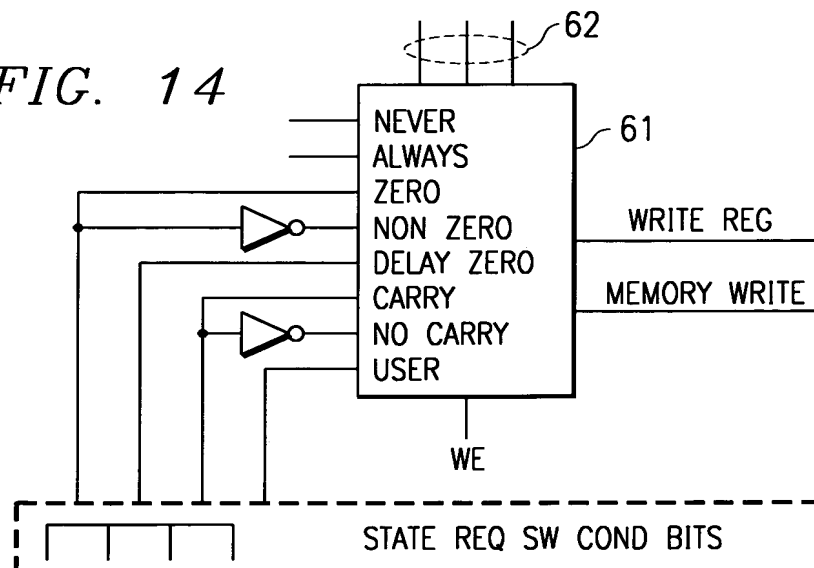


FIG. 13

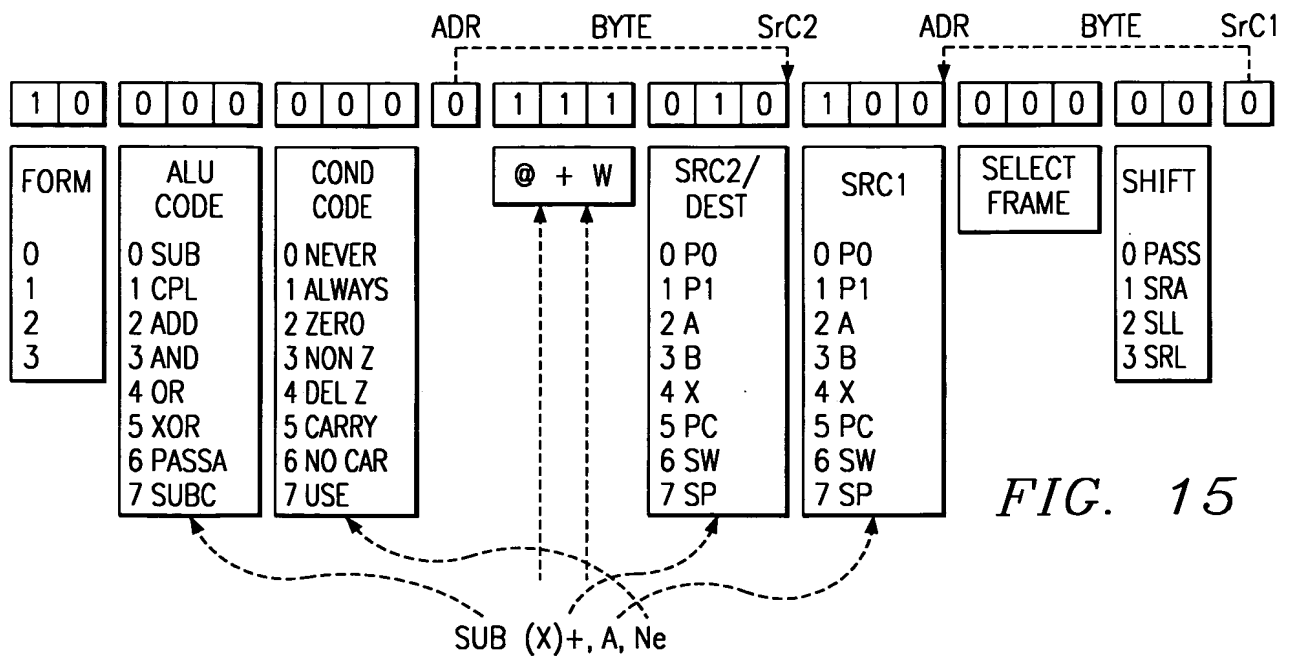
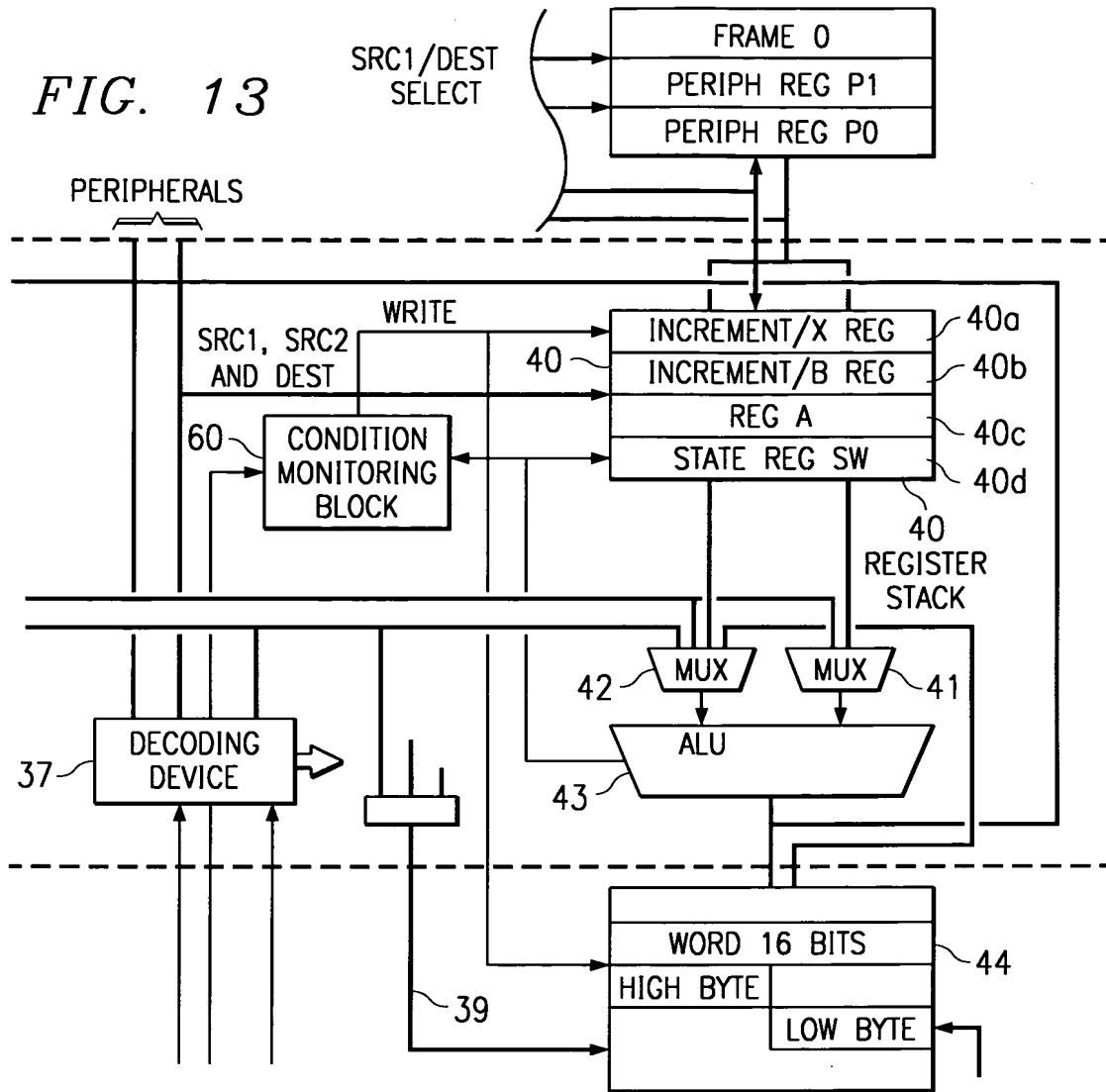


FIG. 15



FIG. 16

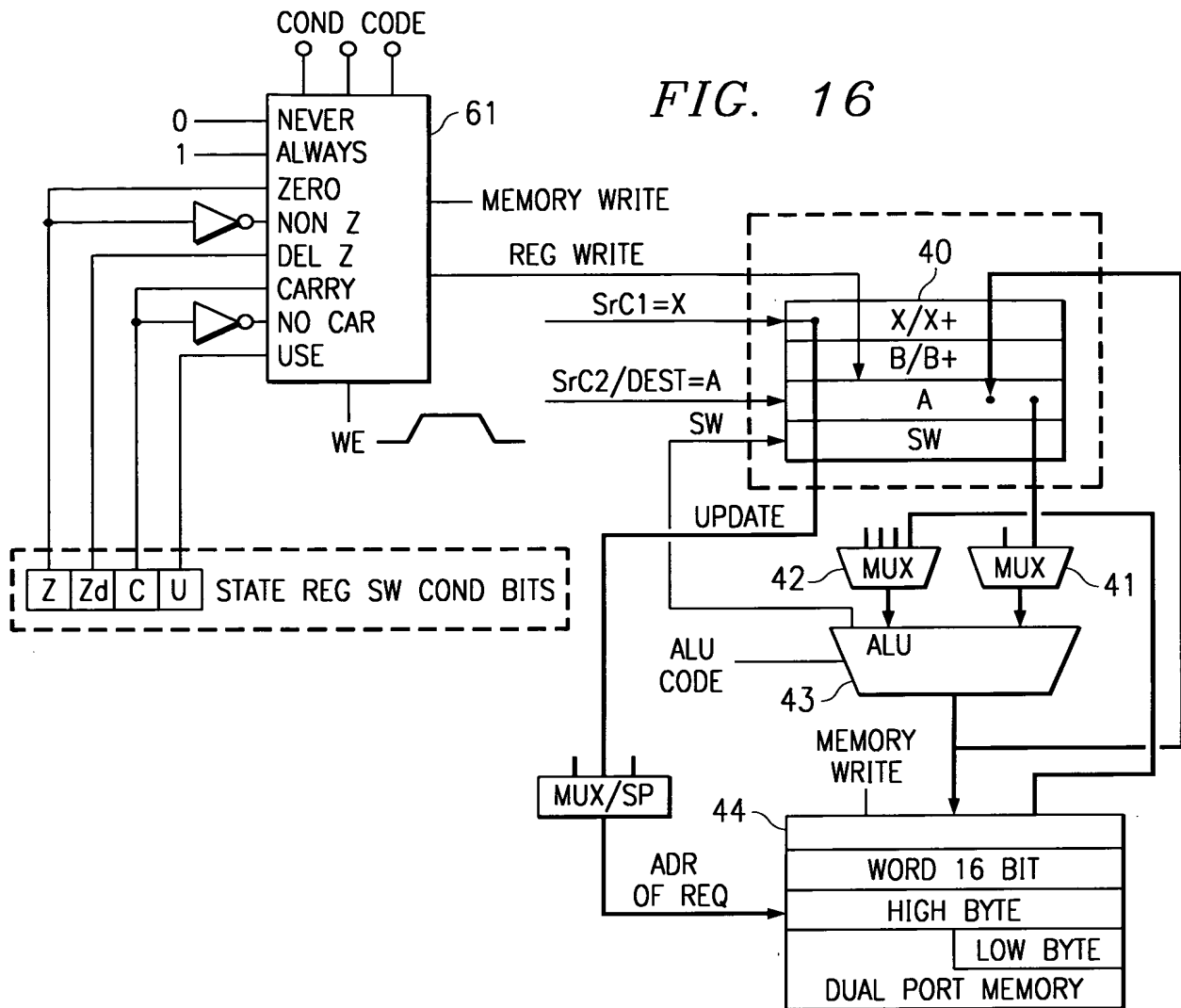


FIG. 17

